

[illegible]

A memory control circuit includes a watching circuit for observing a first request signal from an external device for accessing to a RAM and a second request signal, which has a priority higher than the first request signal, from a CPU for accessing to the RAM. The memory control circuit further includes a control circuit having an OR gate, an AND gate and a NOR gate. When the first and second request signals are inputted, it is scheduled that an operation based on the second access request signal is performed by the control circuit prior to that based on the first access request signal.